Fig. 1

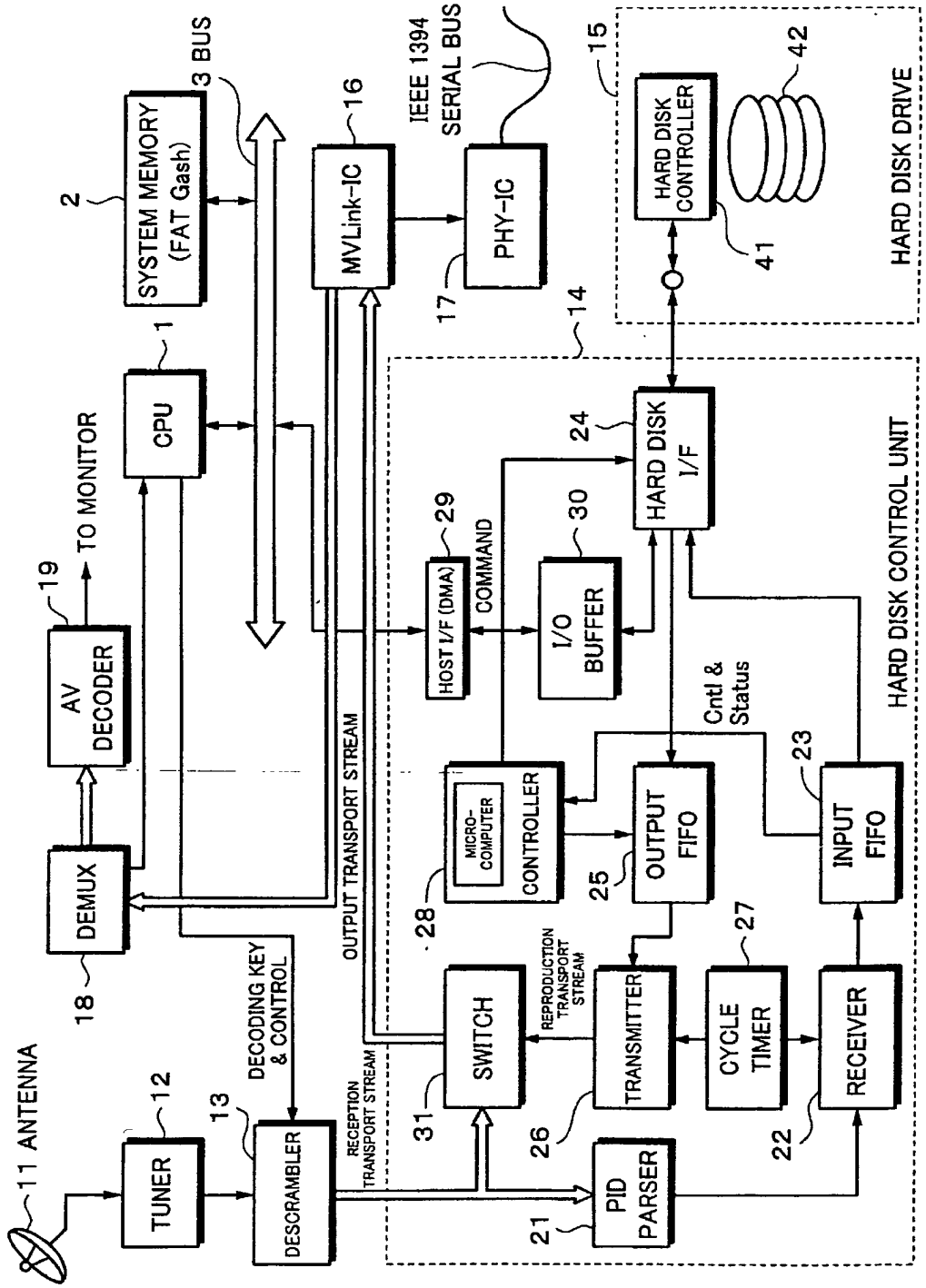


Fig. 2

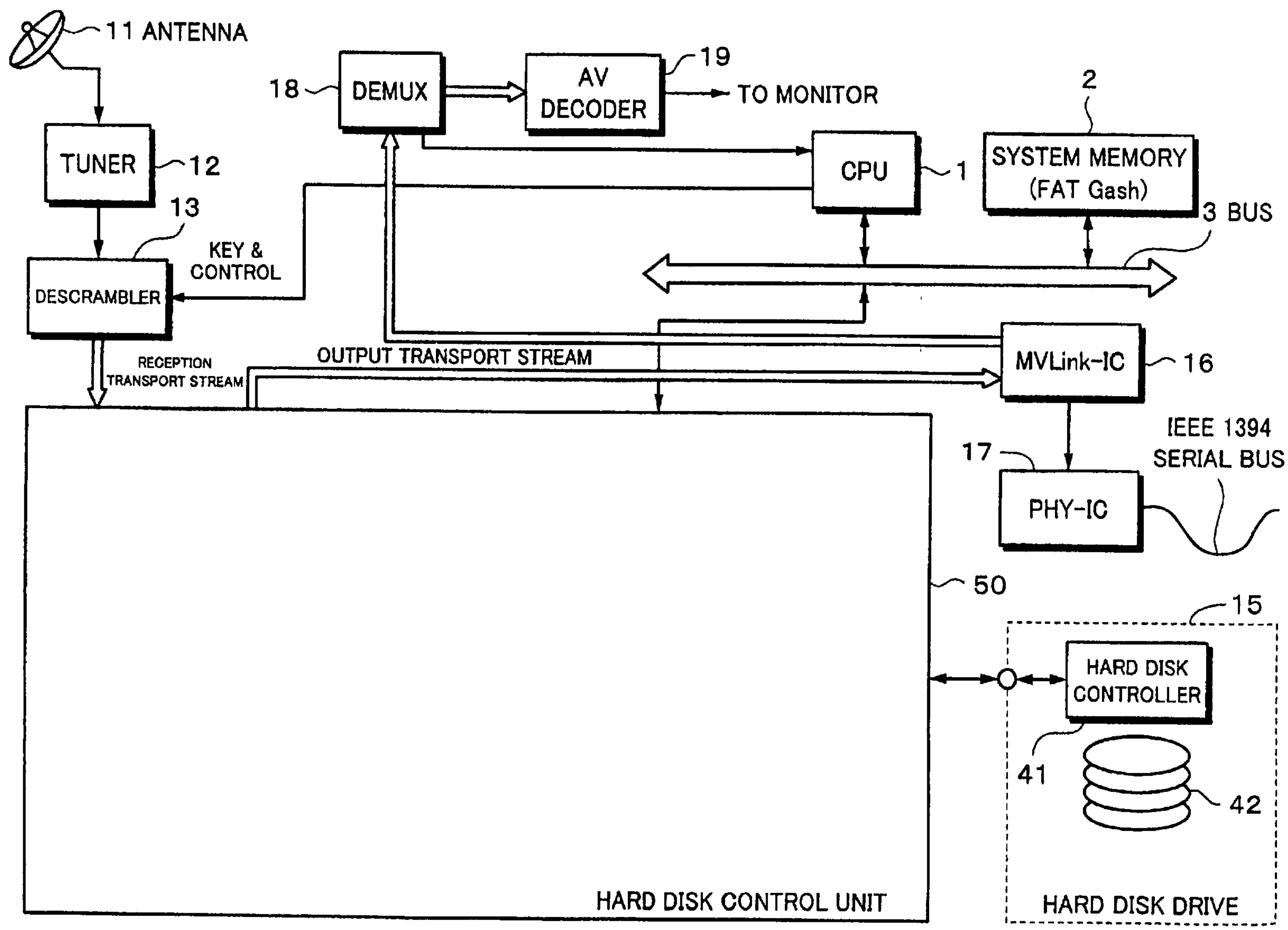

11 ANTENNA
TUNER
12
13
DESCRAMBLER
KEY &
CONTROL
RECEPTION
TRANSPORT STREAM
18
DEMUX
AV
DECODER
19
TO MONITOR
CPU
1
2
SYSTEM MEMORY
(FAT Gash)
3 BUS
OUTPUT TRANSPORT STREAM
MVLink-IC
16
17
PHY-IC
IEEE 1394
SERIAL BUS
50
HARD DISK CONTROL UNIT
15
HARD DISK
CONTROLLER
41
42
HARD DISK DRIVE

Fig. 3

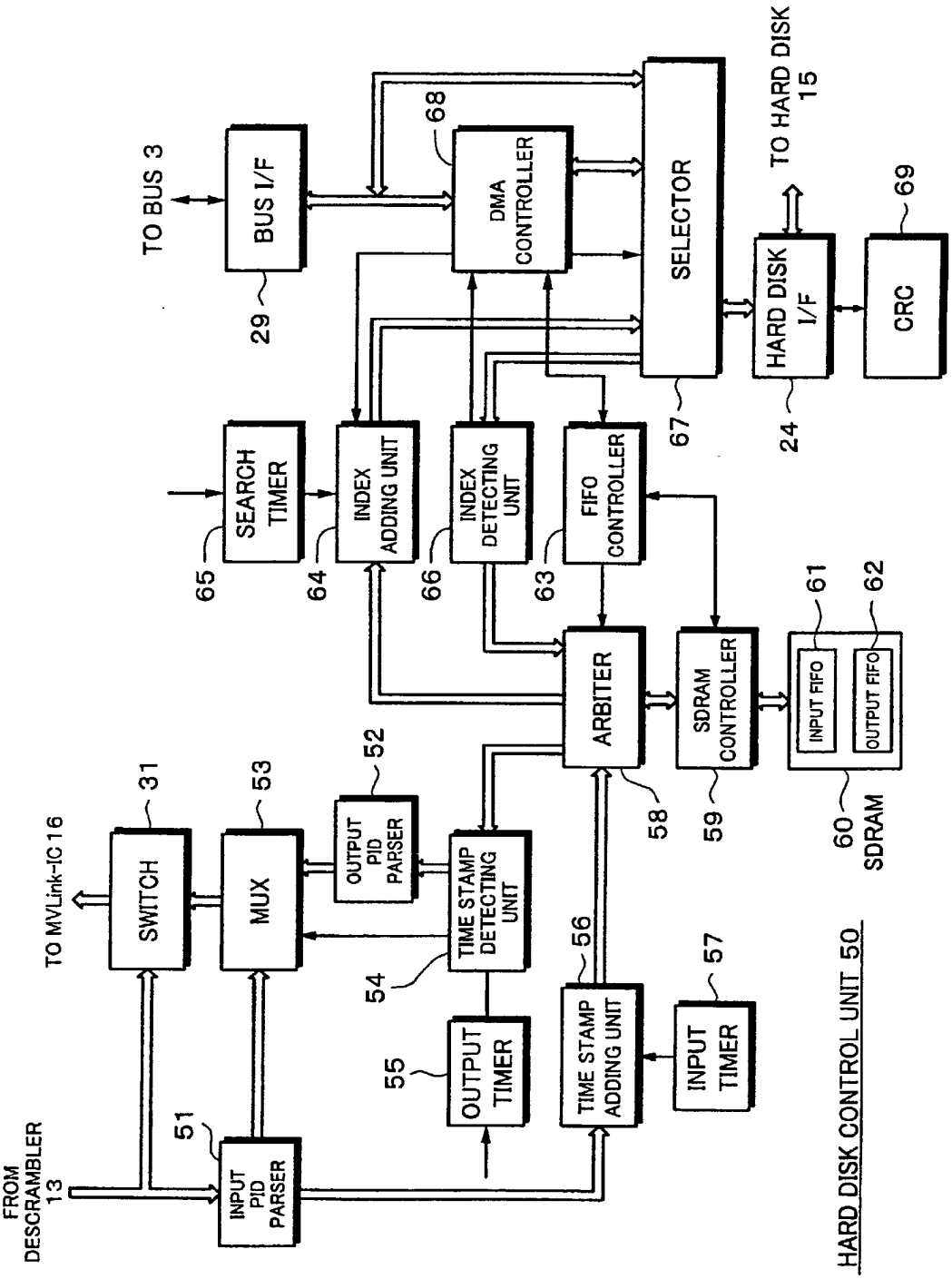


Fig. 4

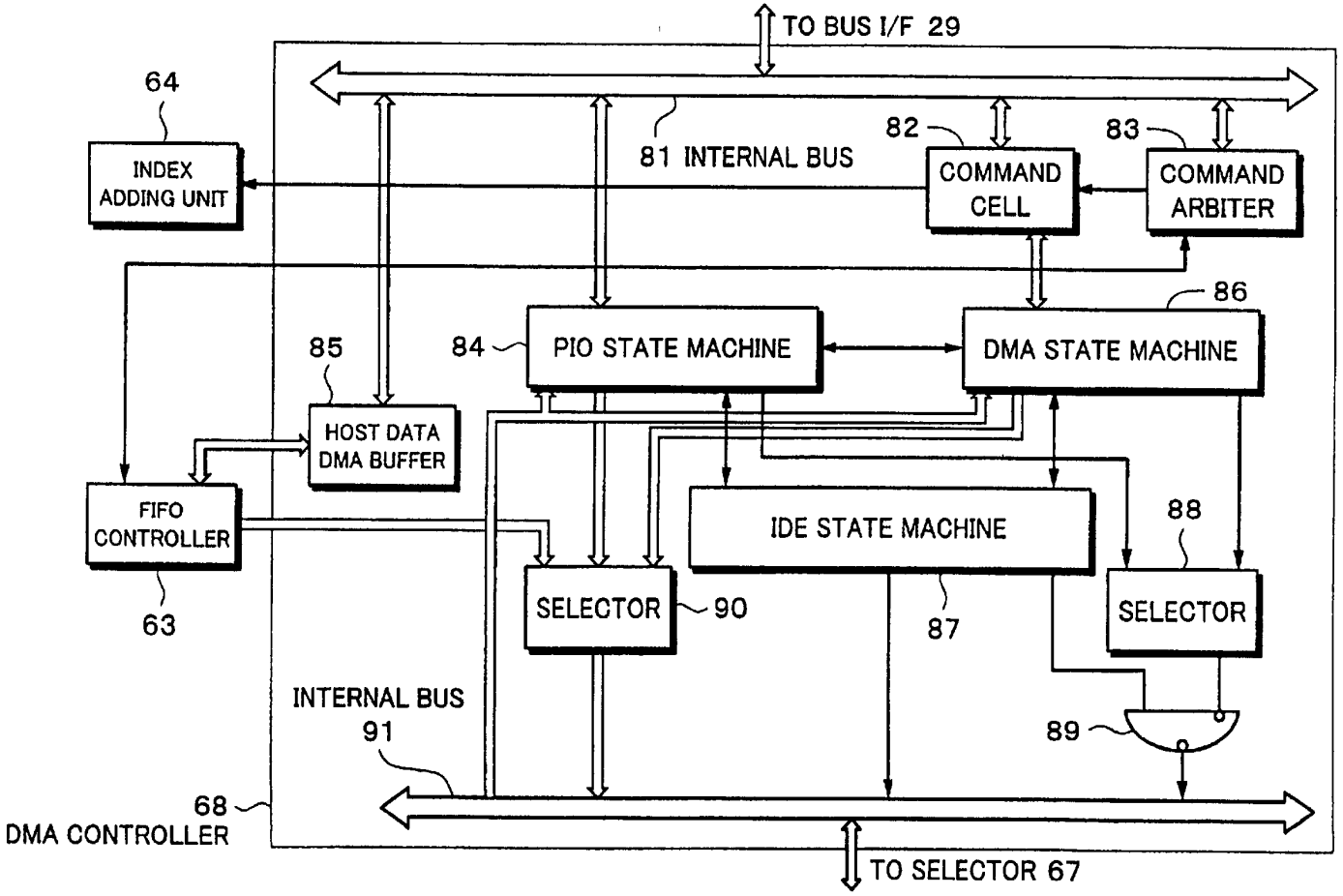

TO BUS I/F 29
64
INDEX ADDING UNIT
81 INTERNAL BUS
82
COMMAND CELL
83
COMMAND ARBITER
86
85
84
PIO STATE MACHINE
DMA STATE MACHINE
HOST DATA DMA BUFFER
FIFO CONTROLLER
63
IDE STATE MACHINE
88
SELECTOR
90
87
SELECTOR
INTERNAL BUS
91
89
68
DMA CONTROLLER
TO SELECTOR 67

Fig. 5

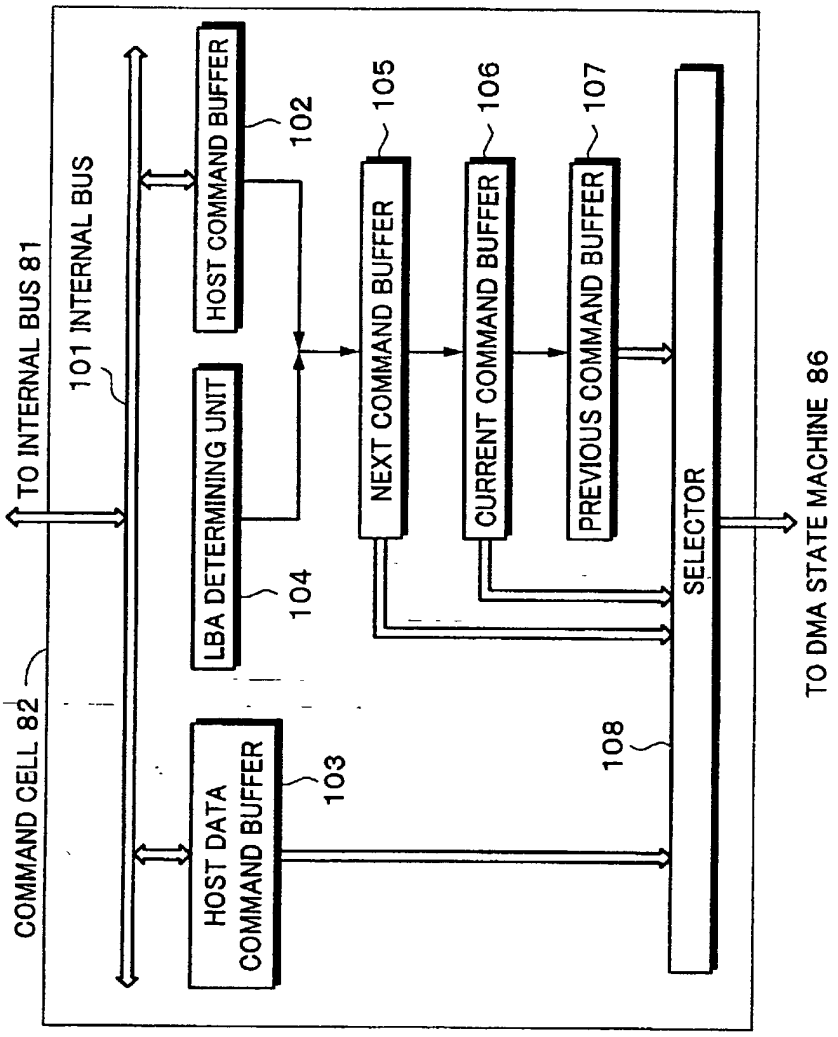


Fig. 6

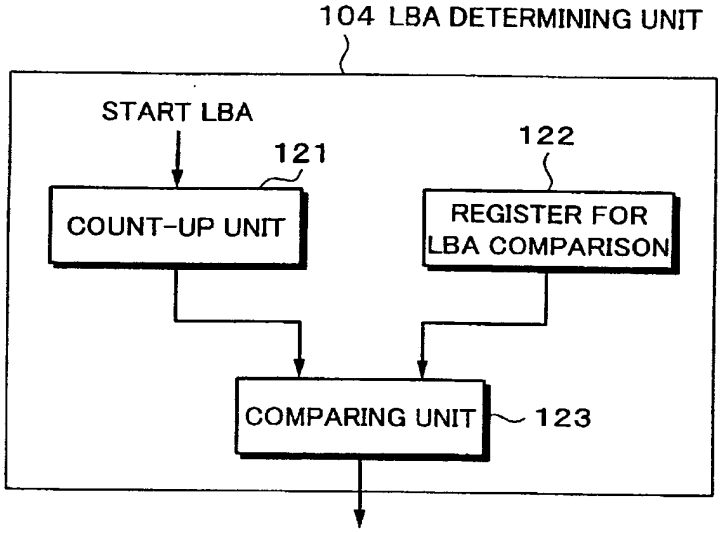

104 LBA DETERMINING UNIT
START LBA
121
122
COUNT-UP UNIT
REGISTER FOR LBA COMPARISON
COMPARING UNIT
123

Fig. 7

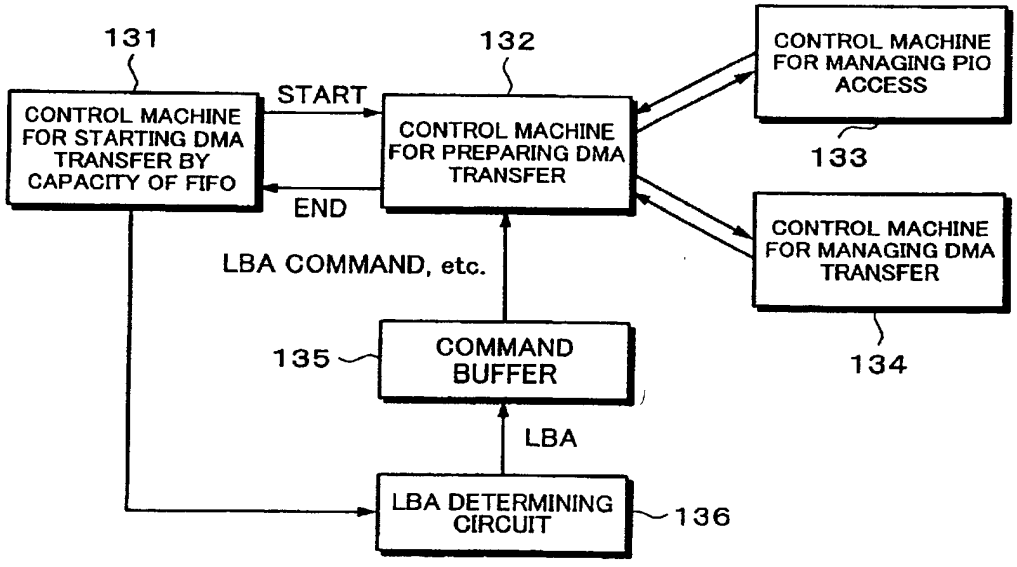

131
132
CONTROL MACHINE FOR STARTING DMA TRANSFER BY CAPACITY OF FIFO
START
END
CONTROL MACHINE FOR PREPARING DMA TRANSFER
CONTROL MACHINE FOR MANAGING PIO ACCESS
133
CONTROL MACHINE FOR MANAGING DMA TRANSFER
134
LBA COMMAND, etc.
135
COMMAND BUFFER
LBA
LBA DETERMINING CIRCUIT
136

Fig. 8

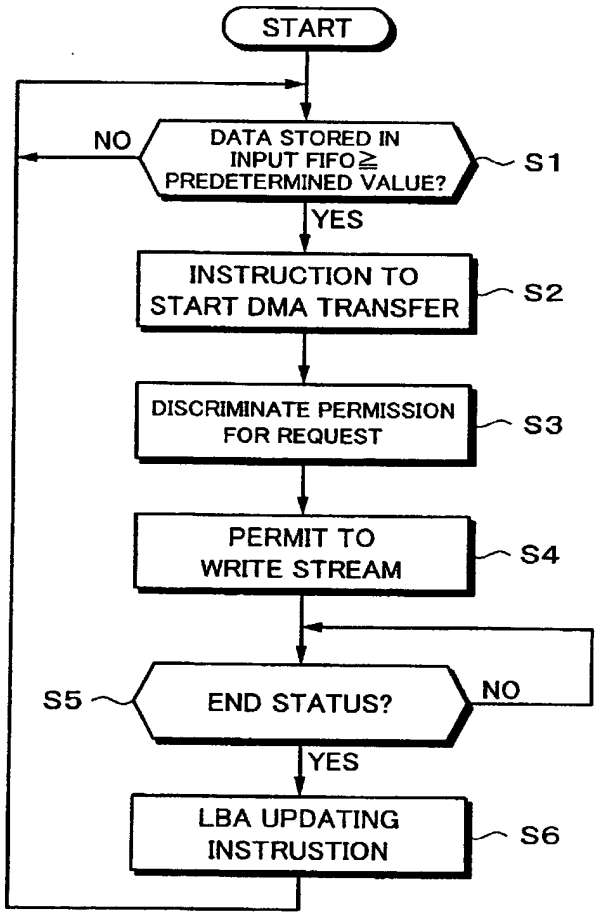

START
NO
DATA STORED IN INPUT FIFO≧ PREDETERMINED VALUE?
S1
YES
INSTRUCTION TO START DMA TRANSFER
S2
DISCRIMINATE PERMISSION FOR REQUEST
S3
PERMIT TO WRITE STREAM
S4
S5
END STATUS?
NO
YES
LBA UPDATING INSTRUSTION
S6

Fig. 9

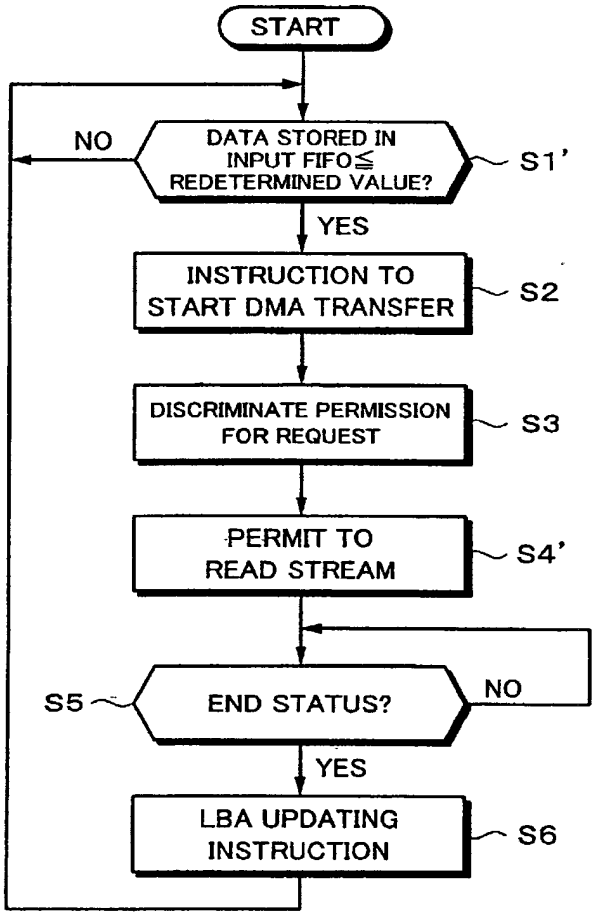
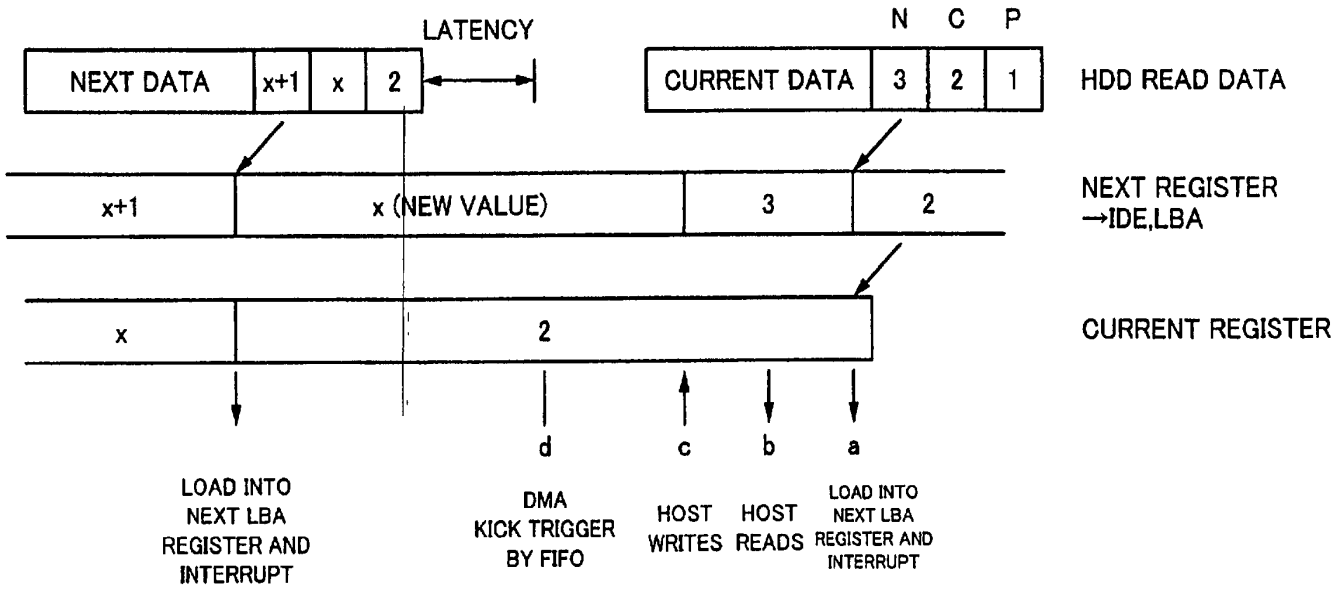


Fig. 10



N: NEXT LBA ADDRESS
C: CURRENT LBA ADDRESS
P: PREVIOUS LBA ADDRESS

Fig. 11

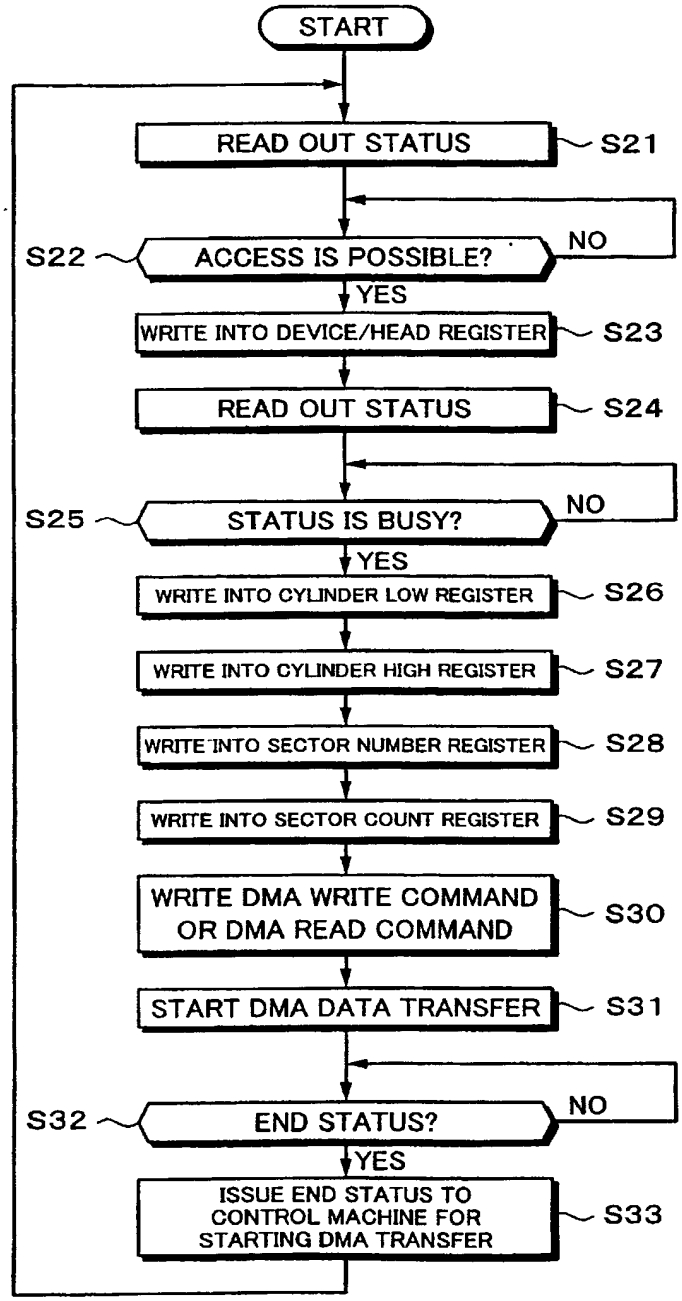

START
READ OUT STATUS
S21
S22
ACCESS IS POSSIBLE?
NO
YES
WRITE INTO DEVICE/HEAD REGISTER
S23
READ OUT STATUS
S24
S25
STATUS IS BUSY?
NO
YES
WRITE INTO CYLINDER LOW REGISTER
S26
WRITE INTO CYLINDER HIGH REGISTER
S27
WRITE INTO SECTOR NUMBER REGISTER
S28
WRITE INTO SECTOR COUNT REGISTER
S29
WRITE DMA WRITE COMMAND OR DMA READ COMMAND
S30
START DMA DATA TRANSFER
S31
S32
END STATUS?
NO
YES
ISSUE END STATUS TO CONTROL MACHINE FOR STARTING DMA TRANSFER
S33

Fig. 12A

ADDRESS (NOTES 1)					REGISTER	
CS1-	CS0-	DA2	DA1	DA0	WRITE	READ
CONTROL BLOCK REGISTER						
L	H	H	H	L	DEVICE·CONTROL	SUBSTITUTE STATUS
L	H	H	H	H	NOT USED	DRIVE ADDRESS
COMMAND BLOCK REGISTER						
H	L	L	L	L	DATA	ERROR
H	L	L	L	H	FEATURE	
H	L	L	H	L	SECTOR·COUNT	
H	L	L	H	H	SECTOR·NO.	
H	L	H	L	L	CYLINDER·LOW	
H	L	H	L	H	CYLINDER·HIGH	
H	L	H	H	L	DEVICE / HEAD	
H	L	H	H	H	COMMAND	STATUS

NOTES 1:BECAUSE CS0- AND CS1 DENOTE NEGATIVE LOGICS L = ASSERT, H = NEGATE

Fig. 12B

b7	b6	b5	b4	b3	b2	b1	b0
RSRV	RSRV	RSRV	RSRV	RSRV	SRST	nIEN	0

RSRV: RESERVATION SRST: SOFTWARE·RESET
nIEN: INTERRUPTION PERMISSION (NEGATIVE LOGIC)

Fig. 12C

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
DATA·BYTE 1 (UPON 16-BIT·ACCESS)								DATA·BYTE 0 (UPON 16-BIT·ACCESS)							
NOT USED (UPON 8-BIT ACCESS)								DATA·BYTE (UPON 8-BIT ACCESS)							

Fig. 12D

b7	b6	b5	b4	b3	b2	b1	b0
SECTOR NO. (CHS MODE)							
LBA BIT (LBA MODE)							

Fig. 13A

CYLINDER・HIGH・REGISTER								CYLINDER・LOW・REGISTER							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
CYLINDER NO. (CHS MODE)															
LBA BIT (LBA MODE)															

Fig. 13B

b7	b6	b5	b4	b3	b2	b1	b0
RSRV	L	RSRV	DEV	HEAD NO. (CHS MODE)			
				LBA BIT (LBA MODE)			

RSRV :RESERVATION
L :LBA MODE SELECTION
DBA :DEVICE ADDRESS

Fig. 13C

b7	b6	b5	b4	b3	b2	b1	b0
THE NUMBER OF SECTORS							

Fig. 13D

b7	b6	b5	b4	b3	b2	b1	b0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

BSY : BUSY (ACCESS INHIBITION)
DRDY : DEVICE・READY
DF : DEVICE・FAULT
DSC : DEVICE・SEEK・ERROR
DRQ : DATA REQUEST
CORR : DATA CORRECTED
IDX : INDEX DETECTION
ERR : ERROR GENERATION

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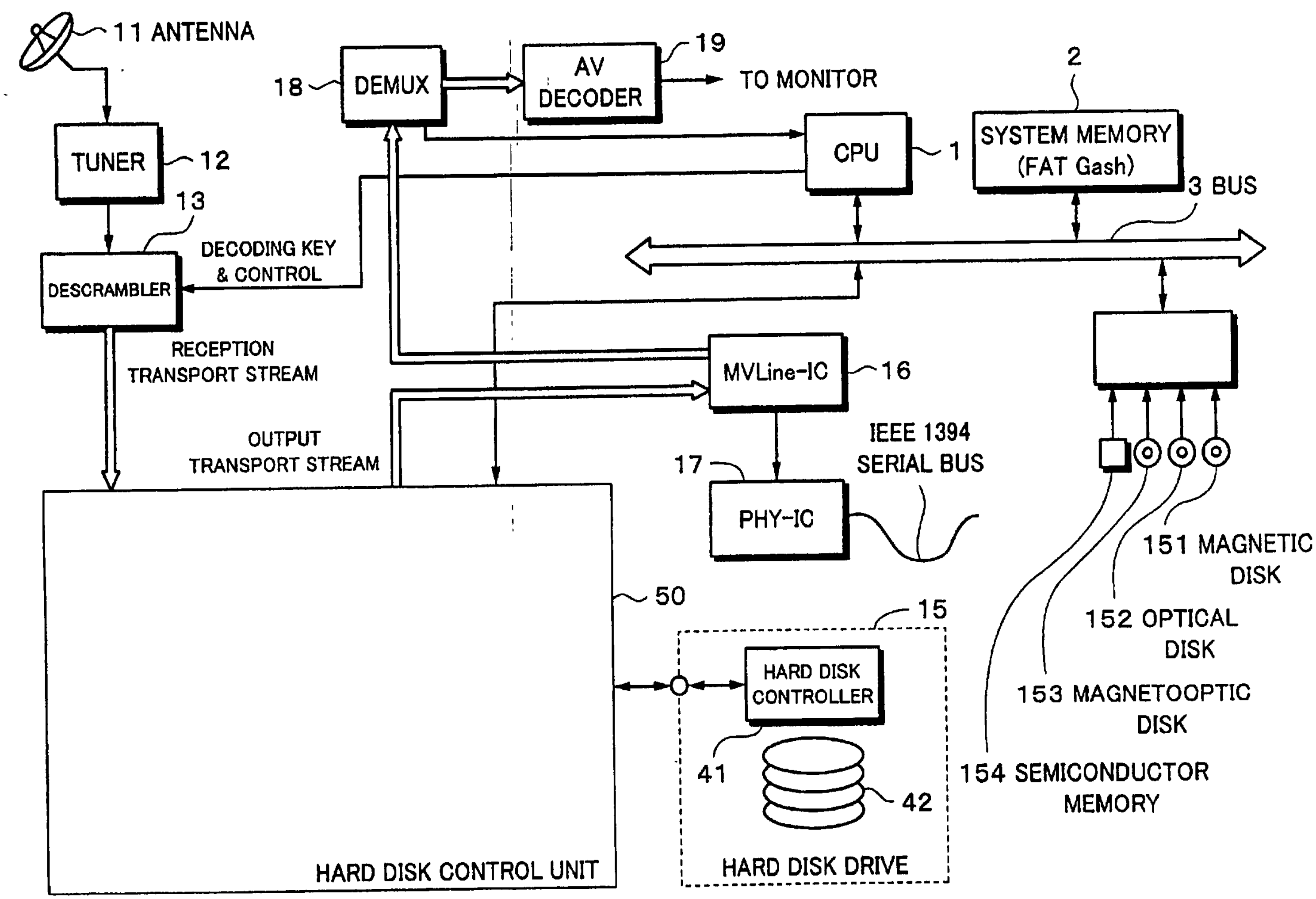
Fig. 14



DESCRIPTION OF REFERENCE NUMERALS

1.. CPU

15.. HARD DISK DRIVE

58.. ARBITER

61.. INPUT FIFO

62.. OUTPUT FIFO

68.. DMA CONTROLLER

82.. COMMAND CELL

104.. LBA DETERMINING UNIT

105.. NEXT COMMAND BUFFER

106.. CURRENT COMMAND BUFFER

107.. PREVIOUS COMMAND BUFFER